

REMARKS**1.Rejection of claims 1-8 under 35 U.S.C. 112:**

5 Claims 1-8 are rejected under 35 USC 112 as the presentation is unclear. Claims appear not to clearly define over the prior art mentioned in the specification and the prior art Figs. Read each term by term on the invention Figs. and discuss patentable
10 novelty vis-a-vis the prior art and the other claims.

Response:

 In the Office Action document, page 4, the Examiner has made a statement of rejection of "Claims 1-87",
15 and it should be "Claims 1-8". Please correct this negligence.

 Claims 1-8 are amended to distinctly define the patentable novelty. Support for the above-mentioned
20 amendment can be found in paragraphs [0023], [0028], and [0029], and Figs.4-5. No new matter is introduced in the amended claims 1-8.

 Additionally, as described in the amended claim
25 1 and Fig.4 of the present application, a gate electrode and a source electrode of each transistor have an overlapping region (i.e. 60a, 60b, and 60c), and further, an area of the overlapping region 60a is smaller than that of the overlapping region 60b, whose
30 area is smaller than that of the overlapping region 60c. That is, an area of an overlapping region between a gate electrode and a source electrode of a transistor

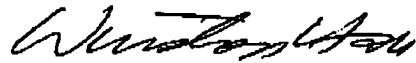
varies with its position in the present application.

However, as described in Fig.3 and paragraph [0011] of the present application, the Applicant Admitted Prior Art discloses that a scanning line 32a and each of the pixel electrodes (i.e. 38a, 38b, and 38c) have an overlapping region (i.e. 40a, 40b, and 40c). Further, the Applicant Admitted Prior Art discloses that an area of an overlapping region 40a is larger than that of the overlapping region 40b, whose area is larger than that of the overlapping region 40c. Accordingly, an area of an overlapping region between a scanning line and a pixel electrode of a pixel varies with its position in the Applicant Admitted Prior Art. The Applicant Admitted Prior Art does not disclose that the gate electrode and the source electrode having an overlapping region and an area of the overlapping region of a pixel closer to the scanning line control circuit is smaller than an area of the overlapping region of another pixel farther from the scanning line control circuit. Therefore, the amended claims are distinct from the Applicant Admitted Prior Art.

Since the Applicant Admitted Prior Art fails to disclose that an area of an overlapping region between a gate electrode and a source electrode of a transistor varies with its position and this feature is explicitly described in the amended claims 1-8 of the present application, the amended claims 1-8 have been clearly defined over the Applicant admitted prior art. Reconsideration of the amended claims 1-8 is courteously solicited.

Accordingly, all claims in the present application, namely, claims 1-8 are now in condition for allowance. Early and favorable indication of
5 allowance is courteously solicited.

10 Sincerely,



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Winston Hsu, Patent Agent No. 41,526

15 P.O. BOX 506

Merrifield, VA 22116

U.S.A.

e-mail : winstonhsu@naipo.com.tw

(Please contact me by e-mail if you need a telephone
20 communication and I will return your call promptly.)